WHAT IS CLAIMED IS:

1. A method of synchronizing a clock signal using a delay lock loop, comprising:

frequency dividing the clock signal to provide a divided signal;

coupling the divided signal to an input of a variable delay circuit, the variable delay circuit outputting a delayed signal;

comparing the divided signal to a phase of the delayed signal to generate a control signal;

applying the control signal to the variable delay circuit to control its delay; and

after a duration, replacing the divided signal at the input of the variable delay circuit with the clock signal.

2. The method of claim 1, further comprising frequency dividing the delayed signal such that the comparing step compares signals of the same frequency.

3. The method of claim 1, wherein the duration is sufficient for enabling the delay lock loop to acquire lock with the divided signal at the input of the variable delay circuit.

4. The method of claim 1, further comprising an initially fixing said control signal to a reset value.

5. The method of claim 4, wherein the reset value sets the variable delay circuit to a minimum setting.

6. The method of claim 1, wherein the variable delay circuit includes a propagation delay.

7. The method of claim 1, wherein the control signal comprises an integrator.

8. The method of claim 1, wherein the control signal comprises a charge pump.

9. The method of claim 1, wherein comparing the divided signal to a phase of the delayed signal to generate a control signal involves assessing the phase difference between the divided signal and the delayed signal.

10. The method of claim 1, wherein the method produces the delayed signal such that it is synchronized with reading or writing of data to and from a memory array.

11. The method of claim 10, further comprising coupling the delayed signal to a vernier circuit to produce various delayed representations of the delayed signal.

12. The method of claim 11, further comprising selecting one of the delayed representations to synchronize the reading and writing.

13. The method of claim 12, wherein selecting is accomplished by a multiplexer.

14. The method of claim 1, wherein replacing the divided signal at the input of the variable delay circuit with the clock signal further comprises dividing the frequency of the delayed signal.

15. A method of locking a delay lock loop in synchronization with a clock signal, comprising:

initializing a variable delay circuit within the delay lock loop to a minimum delay value, wherein the output of the variable delay circuit is coupled to a feedback loop, and wherein delay of the variable delay circuit is controlled by a control signal generated by a feedback loop;

frequency dividing the clock signal and inputting it into the variable delay circuit;

locking the frequency-divided clock signal by adjusting the control signal to the variable delay circuit; and

undividing the frequency-divided clock signal.

16. The method of claim 15, further comprising coupling a frequency divider into the feedback loop after locking.

17. The method of claim 15, wherein the variable delay circuit includes a propagation delay.

18. The method of claim 15, wherein the feedback loop comprises a phase detector for comparing the phase difference between the clock signal and the output of the variable delay circuit.

19. The method of 18, further comprising an integrator coupled to the phase detector for producing the control signal.

20. The method of claim 15, wherein the output of the variable delay circuit is synchronized with reading or writing of data to and from a memory array.

21. The method of claim 20, further comprising coupling the delayed signal to a vernier circuit to produce various delayed representations of the delayed signal.

22. The method of claim 21, further comprising selecting one of the delayed representations to synchronize the reading and writing.

23. The method of claim 22, wherein selecting is accomplished by a multiplexer.

24. A delay lock loop circuit, comprising:

a variable delay circuit configured to receive either a clock signal or a frequency divided version of the clock signal;

a phase detector for receiving as inputs (i) either the output of the variable delay circuit or a frequency divided version of the output of the variable delay circuit, and (ii) the frequency divided version of the clock signal, and for producing a first signal indicative of the phase difference between the two phase detector inputs; and

a feedback loop for receiving the first signal and for producing a control signal;

wherein the control signal is received by the variable delay circuit to adjust the delay of the variable delay circuit.

25. The circuit of claim 24, wherein the variable delay circuit includes a propagation delay.

26. The circuit of 24, wherein the feedback loop comprises an integrator coupled to the first signal for producing the control signal.

27. The circuit of claim 24, wherein the output of the variable delay circuit is synchronized with reading or writing of data to and from a memory array.

28. The circuit of claim 27, further comprising a vernier circuit coupled between the variable delay circuit and the phase detector for producing various delayed representations of the output of the variable delay circuit.

29. The circuit of claim 28, further comprising a multiplexer for selecting one of the delayed representations to synchronize the reading and writing.

30. The circuit of claim 24, further comprising a lock sequencer circuit, wherein the lock sequencer circuit receives a representation of the clock signal and produces a signal to control whether the variable delay circuit receives the clock signal or the frequency divided version of the clock signal.

31. The circuit of claim 24, further comprising a lock sequencer circuit, wherein the lock sequencer circuit receives a representation of the clock signal and produces a signal to control whether the phase detector receives the output of the variable delay circuit or a frequency divided version of the output of the variable delay circuit.

32. The circuit of claim 24, further comprising a lock sequencer circuit, wherein the lock sequencer circuit can interrupt the control signal.

33. The circuit of claim 24, wherein the control signal is resettable to a minimum value.

34. A memory device accessible by a first clock signal, comprising:

a memory array accessible by a second clock signal; and

a delay lock loop for synchronizing the second clock signal with the first clock signal, comprising:

a variable delay circuit for producing the second clock signal, wherein the variable delay circuit is configured to receive either the first clock signal or a frequency divided version of the first clock signal;

a phase detector for receiving as inputs (i) either the second clock signal or a frequency divided version of the second clock signal, and (ii) the frequency divided version of the first clock signal, and for producing a first signal indicative of the phase difference between the two phase detector inputs; and

a feedback loop for receiving the first signal and for producing a control signal;

wherein the control signal is received by the variable delay circuit to adjust the delay of the variable delay circuit.

35. The device of claim 34, wherein the variable delay circuit includes a propagation delay.

36. The device of 34, wherein the feedback loop comprises an integrator coupled to the first signal for producing the control signal.

37. The device of claim 34, further comprising a vernier circuit coupled between the variable delay circuit and the phase detector for producing various delayed representations of the second clock signal.

38. The device of claim 37, further comprising a multiplexer for selecting one of the delayed representations of the second clock signal.

39. The device of claim 34, further comprising a lock sequencer circuit, wherein the lock sequencer circuit receives a representation of the first clock signal and produces a signal to control whether the variable delay circuit receives the first clock signal or the frequency divided version of the first clock signal.

40. The device of claim 34, further comprising a lock sequencer circuit, wherein the lock sequencer circuit receives a representation of the first clock signal and produces a signal to control whether the phase detector receives the second clock signal or a frequency divided version of the second clock signal.

41. The device of claim 34, further comprising a lock sequencer circuit, wherein the lock sequencer circuit can interrupt the control signal.

42. The device of claim 34, wherein the control signal is resettable to a minimum value.

43. A system, comprising:

a microprocessor for producing a first clock signal;

a memory device for receiving the first clock signal, the memory device comprising a memory array accessible by a second clock signal; and

a delay lock loop for synchronizing the second clock signal with the first clock signal, comprising:

a variable delay circuit for producing the second clock signal, wherein the variable delay circuit is configured to receive either the first clock signal or a frequency divided version of the first clock signal;

a phase detector for receiving as inputs (i) either the second clock signal or a frequency divided version of the second clock signal, and (ii) the frequency divided version of the first clock signal, and for producing a first signal indicative of the phase difference between the two phase detector inputs; and

a feedback loop for receiving the first signal and for producing a control signal;

wherein the control signal is received by the variable delay circuit to adjust the delay of the variable delay circuit.

44. The system of claim 43, wherein the variable delay circuit includes a propagation delay.

45. The system of 43, wherein the feedback loop comprises an integrator coupled to the first signal for producing the control signal.

46. The system of claim 43, further comprising a vernier circuit coupled between the variable delay circuit and the phase detector for producing various delayed representations of the second clock signal.

47. The system of claim 46, further comprising a multiplexer for selecting one of the delayed representations of the second clock signal.

48. The system of claim 43, further comprising a lock sequencer circuit, wherein the lock sequencer circuit receives a representation of the first clock signal and produces a signal to control whether the variable delay circuit receives the first clock signal or the frequency divided version of the first clock signal.

49. The system of claim 43, further comprising a lock sequencer circuit, wherein the lock sequencer circuit receives a representation of the first clock signal and produces a signal to control whether the phase detector receives the second clock signal or a frequency divided version of the second clock signal.

50. The system of claim 43, further comprising a lock sequencer circuit, wherein the lock sequencer circuit can interrupt the control signal.

51. The system of claim 43, wherein the control signal is resettable to a minimum value.